IPJ-W1002-A00, IPJ-W1002-C00

Monza® 3 Tag Chip Datasheet

Features

- EPCglobal and ISO 18000-6C compliant, assuring robust performance and seamless interoperability.
- Dual antenna input maximizes range and provides for orientation indifference.
- Superior interference rejection combined with outstanding sensitivity yields excellent tag performance—even when buried deep within a pallet of RF-absorbing material.
- Write rate of >15 tags/second enables rapid programming throughput.
- Commercial temperature range (–40 °C to +85 °C) for reliable performance under harsh conditions.
- Patented interference rejection affords robust performance in noisy environments.
- Impinj's field-rewritable NVM (optimized for RFID) with 96-bit EPC provides programming flexibility and 100,000-cycle/50-year retention reliability.
- Available preprogramming of customer EPCs at the wafer level delivers a fast, reliable, and cost-effective turnkey manufacturing solution.

Overview

The EPCglobal Gen 2 specification is the ultimate standard for automatic identification requirements ranging from items to cases to pallets—worldwide. For supply chain management, inventory control, asset tracking, unique item tracing, product integrity, security, and data accuracy, using fully EPCglobal-compliant, Monza®-powered tags provide the highest level of performance and reliability possible.

Monza tag chips establish new benchmarks for range, readability, and high-speed field rewriteability. And in keeping with Impinj's ground-breaking quality standards, Monza chips are 100% factory tested, with 100,000 cycle/50-year nonvolatile memory retention reliability.

In addition, a supporting family of innovative antenna designs, specifically designed for Monza tag chips, optimizes performance across differing global frequency spectrums and within specialized markets.

Table of Contents

1 Introduction

1.1 Scope

This datasheet defines the physical and logical specifications for Monza tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

EPCglobal™ Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen 2 Specification)
Note: This specification includes normative references, terms and definitions, symbols, abbreviated terms, and notation, the conventions of which were adopted in the drafting of this document.

Impinj Wafer Assembly Specification

Impinj Wafer Map Orientation

EPC™ Tag Data Specification

2 Functional Description

Described are the key functional blocks of the Monza tag silicon, as well as an overview of its operation within a typical application.

2.1 Monza Block Diagram

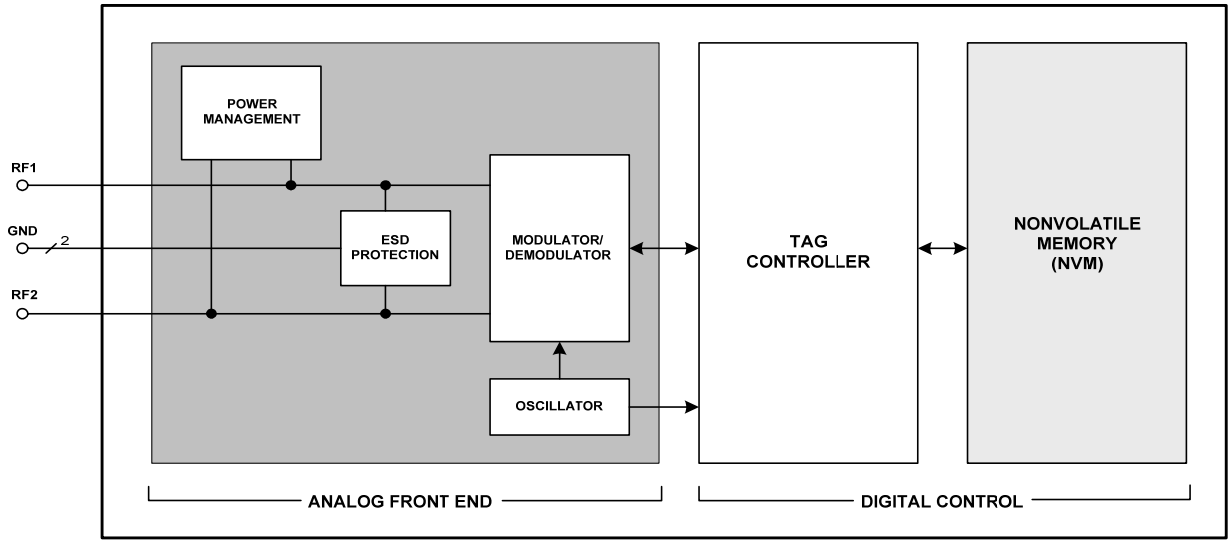


Figure 2-1 Block Diagram

2.2 Pad Descriptions

Monza tag silicon has four external pads available to the user: two antenna pads and two ground pads (the antenna ports are isolated while the ground pads are internally strapped together), as shown in Table 2-1 (see also

Figure 2-2).

Table 2-1 Pad Descriptions

External Signals	External Pad	Description
RF1	1	Antenna Input 1
RF2	1	Antenna Input 2
GND	1	Ground
GND	1	Ground

2.3 Dual Antenna Input

All interaction with Monza tag silicon, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via its two antenna ports and associated grounds.

The dual antenna inputs enable antenna diversity, which in turn minimizes a tag's orientation sensitivity, particularly when the two antennas are of different types (e.g., a combination of loop and dipole) or are otherwise oriented on different axis (X-Y). The dual antenna configuration also enables increased read and write ranges.

The two antenna inputs operate quasi-independently. The power management circuitry receives power from the electromagnetic field induced in the pair, and the demodulator exploits the independent antenna connections, combining the two demodulated antenna signals for processing on-chip.

Monza tag silicon may also be configured to operate using a single antenna port by simply connecting just one of the two inputs. The unused port may be connected to ground (to either, or both ground pads, as they are identical and connected on-chip) or allowed to float. With the exception of the use cases described in section 3.2, the two ports should not be connected to each other, as this will reduce power efficiency.

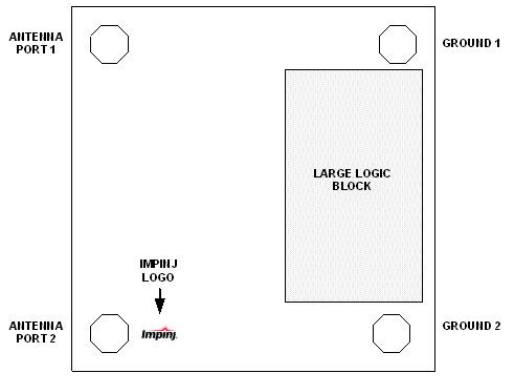


Figure 2-2 Monza die orientation

2.4 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.5 ESD Protection

To divert ESD energy, the ESD Protection block shunts charge from both positive and negative sources when a high voltage is presented across the inputs, thus protecting the chip from damage (see section 5.2).

2.6 Modulator/Demodulator

Monza tag silicon demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.7 Tag Controller

The preceding sections detail the analog functions of power management and signal acquisition and transmission. The Tag Controller block, however, enters the digital domain. While it also performs a number of overhead duties, the heart of this block is the finite state machine logic that carries out the command sequences.

2.8 Nonvolatile Memory

Monza's embedded memory is based on Impinj's multiple-times-programmable (MTP), nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on-chip. Monza NVM provides 100,000 cycle endurance/50-year data retention.

The NVM block is organized into two segments: (1) EPC Memory (up to 96 bits), and (2) Reserved Memory (which contains the Kill and Access passwords). TID Memory is ROM-based, and contains Impinj's manufacturer ID (000000000001) and the Monza model number.

3 Interface Characteristics

Described are the RF interface characteristics of both reader (Forward Link) and tag (Reverse Link).

3.1 Reader-to-Tag (Forward Link) Signal Characteristics

Table 3-1 Forward Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Read Sensitivity Limit		–15		dBm	Input sensitivity is measured on a single RF input at 25 °C. Input sensitivity is specified for a R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25µs, and a T=>R link operating at 256kbps with Miller M=4 encoding.
Write Sensitivity Limit		–11			
Maximum RF Field Strength			+20[1]	dBm	
Modulation Characteristics					
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; Phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth (A-B)/A	80		100	%	
Ripple, Peak-to-Peak M_h=M_l			5	%	Portion of A-B
Rise Time ($t_{r,10\text{-}90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10\text{-}90\%}$)	0		0.33Tari	sec	
Tari[2]	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

Note 1. Reader antenna power with tag chip sitting on antenna. Assumes tag has half-wave dipole antenna. While maximum radiated reader power is +36 dBm for both Read and Write operations, the maximum power the tag should receive is +20 dBm (see section 5.2).

Note 2. Values are nominal; they do not include reader clock frequency error.

3.2 Making Connections

Impinj's patented rectifier technology is realized without the use of diodes. However, the single-ended bridge rectifier model shown in this section serves to illustrate the operating concepts, which are similar. See Section 3.3 for the target source impedance recommended by Impinj for best operation.

3.2.1 Single-ended Connection

In this configuration, the signal is applied between one of the Monza antenna ports and ground. The configuration exhibits the most efficient operation (highest sensitivity) possible, particularly when both RF ports are connected in this fashion. The equivalent rectifier circuit for the single-ended configuration is shown in Figure 3-1 (the portion of the circuit rendered in light gray is not electrically connected).

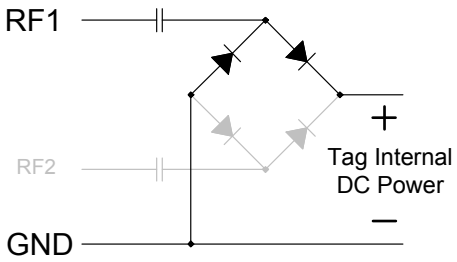


Figure 3-1 Rectifier model, single-ended configuration

Figure 3-2 shows an example of an antenna (Impinj Satellite) designed for connection in this fashion.

Figure 3-2 Antenna designed for single-ended connection. Satellite antenna shown (L), with antenna trace connection detail (R). Note the diagonal pad contacts between RF1 and GND.

The single-ended configuration allows for a variety of possible chip/antenna connections, as shown in Figure 3-3, where the pad locations filled in black are those that are connected to the antenna traces. The dashed gray lines represent the electrical connections within the chip.

Figure 3-3 Chip/antenna connection possibilities for single-ended configuration

Note that Monza tag chips feature two electrically isolated antenna (RF) ports. Thus, a second antenna can be connected in the same single-ended manner, allowing, for example, the use of a dual dipole design, which provides for antenna diversity and enables greater orientation flexibility. The use of Monza's dual antenna inputs also captures more radiated energy, which extends tag read/write range.

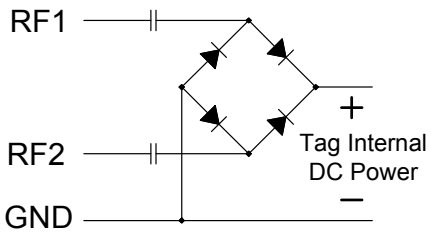


Figure 3-4 Rectifier model, dual single-ended configuration (e.g., dual dipole)

Figure 3-5 Two single-ended connections established for dual dipole antenna. Impinj Jumping Jack tag antenna shown (L) with antenna trace detail (C) and corresponding chip/antenna connections (R).

3.3 Source Impedance

Table 3-2 shows the recommended antenna source impedances for Monza tag silicon across center frequencies of the primary regions of operation (North America, Europe, and Japan) for the single-ended configuration.

Table 3-2 Recommended Antenna Source Impedances

Configuration		Single-ended
Tag silicon Intrinsic Impedance[1]		1529 Ω|| 775fF
Recommended Antenna Impedance[1]	866 MHz	32 + 228j Ω
	915 MHz	32 + 216j Ω
	956 MHz	32 + 207j Ω

Note 1: Values do not include mounting capacitance. Mounting capacitance is dependent on manufacturing tolerance—users should evaluate and determine the appropriate mounting capacitance for their given process

3.4 Reverse Link Signal Characteristics

Table 3-3 Reverse Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $\lvert\Delta\Gamma\rvert$ due to Modulation		0.8			$\lvert\Delta\Gamma\rvert = \lvert\Gamma_{reflect} - \Gamma_{absorb}\rvert$ (per read/write sensitivity, see Table 3-1)
Duty Cycle	45	50	55	%	
Symbol Period[1]	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency[1]	40		640	kHz	

Note 1. Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to arrive at absolute durations and frequencies.

4 Tag Memory

4.1 Monza Memory Map

Table 4-1 depicts both a physical and logical chip memory map. The memory comprises Reserved, EPC, and TID (which is ROM-based, and not user-writable) memory banks.

Table 4-1 Physical/Logical Memory Map

MEM BANK #	MEM BANK NAME	MEM BANK BIT ADDRESS	BIT NUMBER															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10_2	TID (ROM)	10_h-$1F_h$	0	0	0	1	0	0	0	0	1	0	0	1	0	0	1	1
		00_h-$0F_h$	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
01_2	EPC (NVM)	70_h-$7F_h$	EPC[15:0]															
		60_h-$6F_h$	EPC[31:16]															
		50_h-$5F_h$	EPC[47:32]															
		40_h-$4F_h$	EPC[63:48]															
		30_h-$3F_h$	EPC[79:64]															
		20_h-$2F_h$	EPC[95:80]															
		10_h-$1F_h$	PROTOCOL-CONTROL BITS (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	30_h-$3F_h$	ACCESS PASSWORD[15:0]															
		20_h-$2F_h$	ACCESS PASSWORD[31:16]															
		10_h-$1F_h$	KILL PASSWORD[15:0]															
		00_h-$0F_h$	KILL PASSWORD[31:16]															

4.2 Logical vs. Physical Bit Identification

For purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

4.3 Memory Banks

Described in the following sections are the contents of the NVM and ROM memory, and the parameters for their associated bit settings.

4.3.1 Reserved Memory

Reserved Memory contains the *Access* and *Kill* passwords.

4.3.2 Passwords

Monza tag chips have a 32-bit Access Password and 32-bit Kill Password. The default password for both Kill and Access is $00000000_{h.}$

4.3.3 Access Password

The Access Password is a 32-bit value stored in Reserved Memory 20_h to $3F_h$ MSB first. The default value is all zeroes. Tags with a non-zero Access Password will require a reader to issue this password before transitioning to the secured state. A tag that does not implement an Access Password acts as though it had a zero-valued Access Password that is permanently read/write locked.

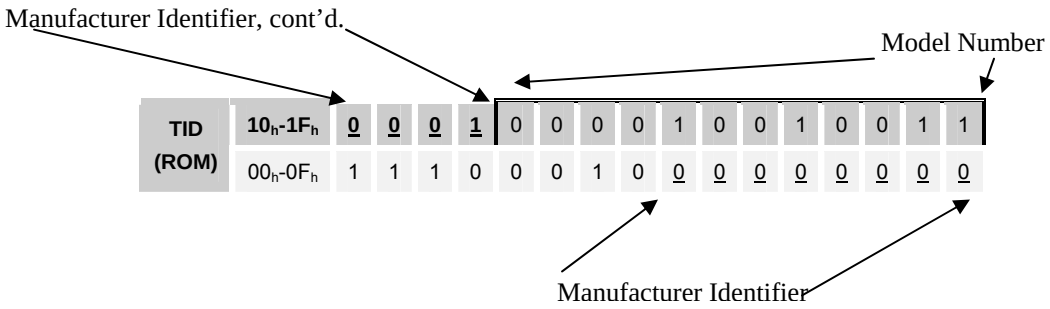
4.3.4 Kill Password

The Kill Password is a 32-bit value stored in Reserve Memory 00_h to $1F_{h,}$ MSB first. The default value is all zeroes. A reader shall use a tag's kill password once to kill the tag and render it silent thereafter. A tag will not execute a kill operation if its Kill Password is all zeroes. A tag that does not implement a Kill Password acts as though it had a zero-valued Kill Password that is permanently read/write locked.

4.3.5 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The Impinj MDID (Manufacturer Identifier) is 0x001 (shown in Table 4-1as the underlined bits that cross both TID memory map rows). The Monza model number is shown in Table 4-1 as the bits outlined in double black lines (0x093) in TID memory row 10_h-$1F_h$. The non-shaded bit locations in TID row 00_h-$0F_h$ store the EPCglobal™ Class ID (0xE2). See Table 4-2 for detail.

Table 4-2 TID Detail



4.3.6 EPC Memory

EPC memory contains the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$, a CRC16 at memory addresses 00_h to $0F_h$, and an EPC value beginning at address 20_h. A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command, and providing a memory address using the extensible-bit-vector (EBV) format. The PC, CRC16, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

The EPC written at time of manufacture is as shown in Table 4-3.

Table 4-3 EPC Preprogramming Detail

Impinj Part Number	96-Bit EPC Value Preprogrammed at Manufacture (hex)
IPJ-W1002-A00 IPJ-W1002-C00	3008 33B2 DDD9 06C0 0000 0000

5 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 5-1 lists the ranges that will be referred to in this specification. Tag chip functional and performance requirements are met over the operating range, unless otherwise specified.

Table 5-1 Temperature parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Extended Operating Temperature	–40		+85	°C	Default range for all functional and performance requirements
Storage Temperature	–40		+85	°C	
Assembly Survival Temperature			+150	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Input Damage Levels

The tag chip is guaranteed to survive the inputs specified in Table 5-2.

Table 5-2 ESD and input limits

Parameter	Minimum	Typical	Maximum	Units	Comments
ESD			2,000	V	HBM (Human Body Model)
Reader antenna power with tag sitting on antenna			36[1]	dBm	Tag has 10 cm half-wave dipole antenna
DC input voltage			± 3.5	volts	Applied across two pads
DC input current			± 0.5	mA	Into any input pad

Note 1. Assumes tag has half-wave dipole antenna. While maximum radiated reader power is +36 dBm for both Read and Write operations, the maximum power the tag should receive is +20 dBm (see Table 3-1).

5.3 NVM Use Model

The Monza tag chip memory has 100,000 write cycles/50-year data retention reliability.

6 Ordering Information

Part Number	Form	Product	Processing Flow
IPJ-W1002-A00	Wafer	Monza	Raw: non-bumped, non-thinned
IPJ-W1002-C00	Wafer	Monza	Bumped, thinned (to 6 mils, or ~150 µm), and sawn

Notices:

www.impinj.com